

10/091792

03/06/02

PATENT NUMBER and  
ISSUE DATE

## U.S. UTILITY Patent Application

APPL NUM 10091792	FILING DATE 03/06/2002	CLASS 338	SUBCLASS 610.1 3.08	GAU 2832	EXAMINER S. J. H. [Signature]
<b>**APPLICANTS:</b> Huber Louis; Shoshani Ziv; 3729					
<b>**CONTINUING DATA VERIFIED:</b> THIS APPLICATION IS A DIV OF 09/811,844 03/19/2001					
<b>** FOREIGN APPLICATIONS VERIFIED:</b>					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO P04870US1	
Verified and Acknowledged Examiners's initials					
TITLE : Method for manufacturing a power chip resistor					

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436 (Rev. 12-94)

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Total Claims	Print Claim for O.G.
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
<input type="checkbox"/> <b>TERMINAL</b>		<b>Application Examiner</b>	
<b>DISCLAIMER</b>		<b>PREPARED FOR ISSUE</b>	
<b>WARNING:</b> The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code, Title 35, Sections 122, 181 and 188. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.			

FILED WITH:

☐ DISK (CRF)☐ CD-ROM

(Attached in pocket on right inside flap)